**What is LEF mean?**

LEF is an ASCII data format from Cadence Design Inc. to describe a standard cell library.

It includes the design rules for routing and the Abstract layout of the cells. LEF file contains the following,

Technology: layer, design rules, via-definitions, metal-capacitance.

Site: Site extension

Macros: cell descriptions, cell dimensions, layout of pins and blockages, capacitances

**What is DEF mean?**

DEF is an ASCII data format from Cadence Design Inc., to describe Design related information.

**Steps involved in designing an optimal pad-ring**

1. Make sure you have corner-pads, across all the corners of the pad-ring. The corners of the pad ring just connect the power and ground rings that run through the pads. This is mainly to have the power-continuity as well as the resistance is low.

2. Ensure that the Pad-ring full-fills the ESD requirement. Identify the power-domains, split the domains, Ensure common ground across all the domains.

3. Ensure the pad-ring has full-filled the SSN (Simultaneous Switching Noise) requirement.

4. Placing Transfer-cell Pads in the cross power-domains, for different height pads, to have rail connectivity.

5. Ensure that the design has sufficient core power-pads.

6. Choose the Drive-strength of the pads based on the current requirements, timing.

7. Ensure that there is separate analog ground and power pads.

8. A No-Connection Pad is used to fill out the pad-frame if there is no requirement for I/O's. Extra VDD/GND pads also could be used. Ensure that no Input/output pads are used with un-connected inputs, as they consume power if the inputs float.

9. Ensure that oscillator-pads are used for clock inputs.

10. In-case if the design requirement for source synchronous circuits, make sure that the clock and data pads are of same drive-strength.

11. Breaker-pads are used to break the power-ring, and to isolate the power-structure across the pads.

12. Ensure that the metal-wire connected to the pin can carry sufficient amount of the current, check if more than one metal-layer is necessary to carry the maximum current provided at the pin.

**What is IR drop? How to avoid? How it affects timing?**

There is a resistance associated with each metal layer. This resistance consumes power causing voltage drop i.e.IR drop. If IR drop is more ==> delay increases.

**How will you decide the die size?**

By checking the total area of the design you can decide die size.

**If lengthy metal layer is connected to diffusion and poly, then which one will affect by antenna problem?**

Poly

**If the full chip design is routed by 7 layer metal, why macros are designed using 5LM instead of using 7LM?**

Because top two metal layers are required for global routing in chip design. If top metal layers are also used in block level it will create routing blockage.

**In your project what is die size, number of metal layers, technology, foundry, number of clocks?**

Die size: tell in mm eg. 1mm x 1mm ; remember 1mm=1000micron which is a big size !!

Metal layers: See your tech file. Generally for 90nm it is 7 to 9. In 90nm Vdd = 1.2, Vthn = 0.18v

**What is SDC constraint file contains?**

Clock definitions, Timing exception-multi cycle path, false path, Input and Output delays

**How did you do power planning? How to calculate core ring width, macro ring width and strap or trunk width? How to find number of power pad and IO power pads? How the width of metal and number of straps calculated for power and ground?**

Get the total core power consumption; get the metal layer current density value from the tech file; Divide total power by number sides of the chip; Divide the obtained value from the current density to get core power ring width. Then calculate number of straps using some more equations. Will be explained in detail later.

**What is logic optimization and give some methods of logic optimization.**

Upsizing, Downsizing, Buffer insertion, Buffer relocation, Dummy buffer placement

**What is electromigration (EM) and it effects?**

Due to high current flow in the metal atoms of the metal can displaced from their original place. When it happens in larger amount the metal can open or bulging of metal layer can happen. This effect is known as electromigration.

Affects: Either short or open of the signal line or power line.

**What is cloning and buffering?**

Cloning is a method of optimization that decreases the load of a heavily loaded cell by replicating the cell.

Buffering is a method of optimization that is used to insert buffers in high fan out nets to decrease the delay.

**Time-dependent gate oxide breakdown** (or **time-dependent dielectric breakdown**, **TDDB**)

It is a failure mechanism in [MOSFETs](http://en.wikipedia.org/wiki/Metal–Oxide–Semiconductor_Field-Effect_Transistor), when the [gate oxide](http://en.wikipedia.org/wiki/Gate_oxide) [breaks down](#Failure_of_electrical_insulation) as a result of long-time application of relatively low electric field (as opposite to immediate breakdown, which is caused by strong electric field). The breakdown is caused by formation of a conducting path through the gate oxide to [substrate](http://en.wikipedia.org/wiki/Wafer_(electronics)) due to electron [tunneling](http://en.wikipedia.org/wiki/Quantum_tunnelling) current, when MOSFETs are operated close to or beyond their specified operating voltages.

**What is Netlist?**   
Netlists usually convey connectivity information and provide nothing more than instances, nets, and perhaps some attributes. An "instance" could be anything from a [MOSFET](http://en.wikipedia.org/wiki/MOSFET) transistor or a bipolar transistor, to a [resistor](http://en.wikipedia.org/wiki/Resistor), [capacitor](http://en.wikipedia.org/wiki/Capacitor), or [integrated circuit](http://en.wikipedia.org/wiki/Integrated_circuit) chip.

**What is Different Types of IC packaging?**   
ICs are packaged in many types they are:

\* BGA1  
\* BGA2  
\* Ball grid array  
\* CPGA  
\* Ceramic ball grid array  
\* Cerquad  
\* DIP-8  
\* Die attachment  
\* Dual Flat No Lead  
\* Dual in-line package  
\* Flat pack  
\* Flip chip  
\* Flip-chip pin grid array  
\* HVQFN  
\* LQFP  
\* Land grid array  
\* Leadless chip carrier  
\* Low insertion force  
\* Micro FCBGA  
\* Micro Lead frame Package  
\* Micro Lead Frame  
\* Mini-Cartridge  
\* Multi-Chip Module  
\* OPGA  
\* PQFP  
\* Package on package  
\* Pin grid array  
\* Plastic leaded chip carrier  
\* QFN  
\* QFP  
\* Quadruple in-line package  
\* ROM cartridge  
\* Shrink Small-Outline Package  
\* Single in-line package  
\* Small-Outline Integrated Circuit  
\* Staggered Pin Grid Array  
\* Surface-mount technology  
\* TO220  
\* TO3  
\* TO92  
\* TQFP  
\* TSSOP  
\* Thin small-outline package  
\* Through-hole technology  
\* UICC  
\* Zig-zag in-line package  
  
**How does Resistance of the metal lines vary with increasing thickness and increasing length?**